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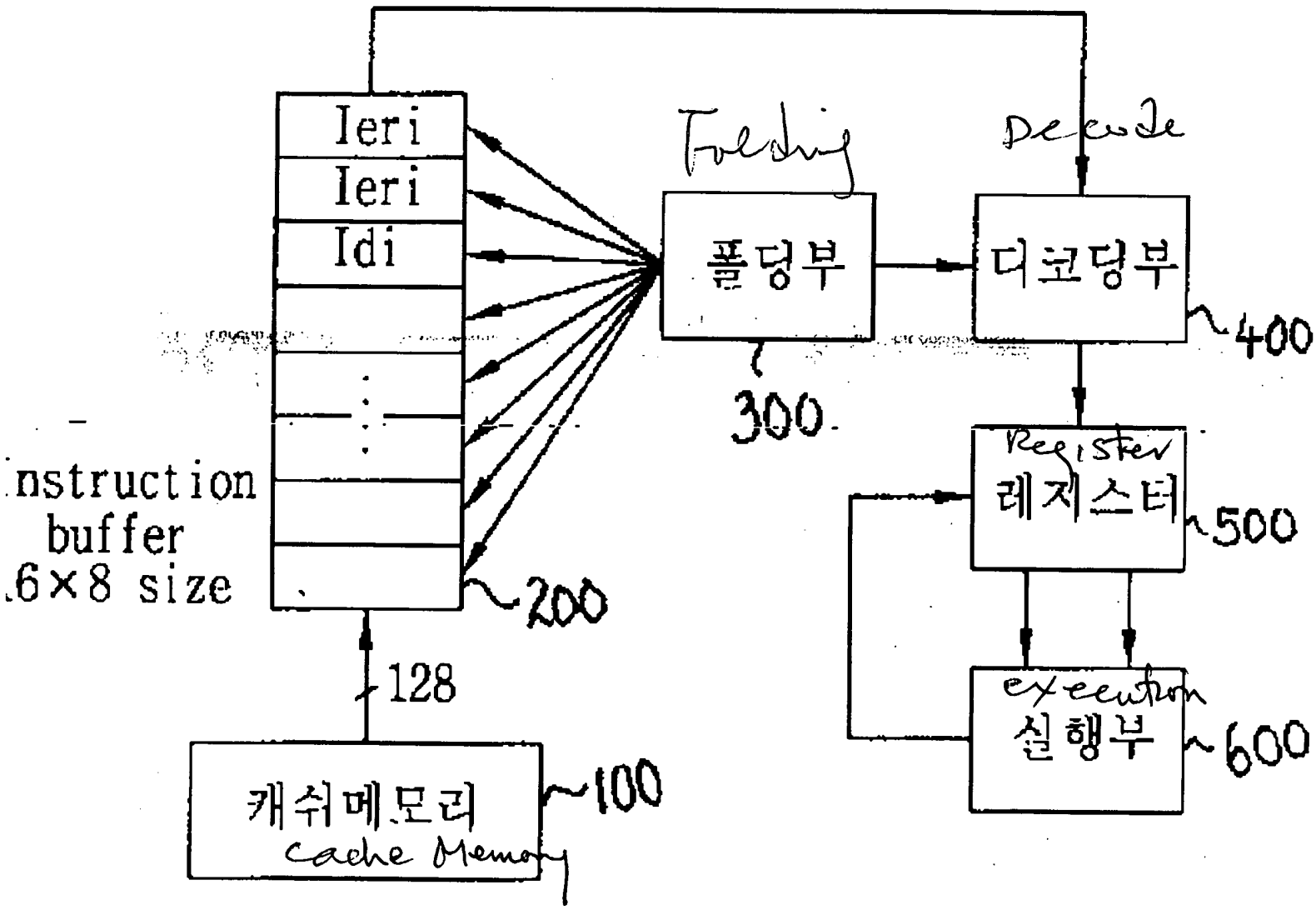

US005398321A

United States Patent [19]

Jeremiah

[11] Patent Number: 5,398,321

[45] Date of Patent: Mar. 14, 1995

[54] MICROCODE GENERATION FOR A SCALABLE COMPOUND INSTRUCTION SET MACHINE

[75] Inventor: Thomas L. Jeremiah, Endwell, N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 184,401

[22] Filed: Jan. 21, 1994

Related U.S. Application Data

[63] Continuation of Ser. No. 653,006, Feb. 8, 1991, abandoned.

[51] Int. Cl.[6] G06F 9/22; G06F 9/38

[52] U.S. Cl. 395/375; 364/DIG. 1; 364/DIG. 2; 364/231.8; 364/230; 364/931.41; 364/946.9; 364/948.3; 364/262.4

[58] Field of Search 395/375

[56] References Cited

U.S. PATENT DOCUMENTS

4,295,193	10/1981	Pomerene	395/375
4,376,976	3/1983	Lahti et al.	395/375
4,439,828	3/1984	Martin	364/200
4,594,655	6/1986	Hao et al.	395/775
4,825,363	4/1989	Baumann et al.	395/375
4,858,105	8/1989	Kuriyama et al.	395/375
4,942,525	7/1990	Shintani et al.	395/375
4,967,343	10/1990	Ngai et al.	395/800
5,005,118	4/1991	Lenoski	395/375
5,051,940	9/1991	Vassiliadis et al.	364/736
5,117,490	5/1992	Duxbury et al.	395/375
5,129,067	7/1992	Johnson	395/375
5,140,545	8/1992	Vassiliadis et al.	364/765
5,155,819	10/1992	Watkins et al.	395/375
5,163,139	11/1992	Haigh et al.	395/375
5,229,321	2/1993	Iizuka	395/375
5,241,636	8/1993	Kohn	395/375
5,287,467	2/1994	Blaner et al.	395/375
5,295,249	3/1994	Blaner et al.	395/375
5,299,319	3/1994	Vassiliadis et al.	395/375
5,301,341	4/1994	Vassiliadis et al.	395/800
5,303,356	4/1994	Vassiliadis	395/375

FOREIGN PATENT DOCUMENTS

0045634	2/1982	European Pat. Off. .
0184158	6/1986	European Pat. Off. .
0397414	11/1990	European Pat. Off. .
2293932	12/1990	Japan .

OTHER PUBLICATIONS

Acosta, R. D., et al, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors", IEEE Transactions on Computers, Fall, C-35 No. 9, Sep. 1986, pp. 815–828.

Anderson, V. W., et al, the IBM System/360 Model 91: "Machine Philosophy and Instruction Handling", computer structures: Principles And Examples (Siewiorek, et al, ed (McGraw-Hill, 1982, pp.276–292.

Capozzi, A. J., et al, "Non-Sequential High-Performance Processing" IBM Technical Disclosure Bulletin, vol. 27, No. 5, Oct. 1984, pp. 2842–2844.

Chan, S., et al, "Building Parallelism into the Instruction Pipeline", High Performance Systems, Dec., 1989, pp. 53–60.

(List continued on next page.)

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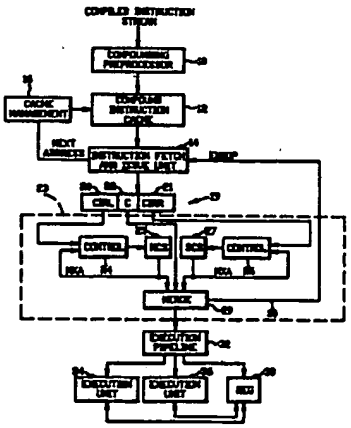
Attorney, Agent, or Firm—Lynn L. Augspurger; Terrance A. Meador

[57] ABSTRACT

An apparatus for generating microcode in a scalable compound instruction set machine operates in response to compounding information indicating that two or more adjacent instructions are to be executed in parallel. Separate and independent microcode is held in control store for each possible instruction in a group. Microcode sequences for each instruction of a group of instructions to be executed in parallel are merged in response to the compounding information into a single microinstruction sequence.

9 Claims, 7 Drawing Sheets



US005197135A

United States Patent [19]

Eickemeyer et al.

[11] Patent Number: 5,197,135

[45] Date of Patent: Mar. 23, 1993

[54] MEMORY MANAGEMENT FOR SCALABLE COMPOUND INSTRUCTION SET MACHINES WITH IN-MEMORY COMPOUNDING

[75] Inventors: Richard J. Eickemeyer, Endicott; Stamatis Vassiliadis, Vestal; Bartholomew Blaner, Newark Valley, all of N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 543,458

[22] Filed: Jun. 26, 1990

[51] Int. Cl.[5] G06F 9/38

[52] U.S. Cl. 395/375; 395/800; 364/DIG. 1; 364/262.4; 364/262.9; 364/263; 364/261; 364/261.1; 364/261.2

[58] Field of Search 395/375, 800, 775, 650

[56] References Cited

U.S. PATENT DOCUMENTS

4,439,828	3/1984	Martin	364/200
4,466,057	8/1984	Houseman et al.	395/375
4,722,049	1/1988	Lahti	395/375
5,086,408	2/1992	Sakata	395/600

OTHER PUBLICATIONS

Acosta, R. D., et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors", IEEE Transactions on Computers, Fall, C-35, No. 9, Sep. 1986, pp. 815-828.

Anderson, V. W., et al, the IBM System/360 Model 91: "Machine Philosophy and Instruction Handling", computer structures: Principles and Examples (Siewiorek, et al, ed (McGraw-Hill, 1982, pp. 276-292.

Capozzi, A. J., et al, "Non-Sequential High-Performance Processing", IBM Technical Disclosure Bulletin, vol. 27, No. 5, Oct. 1984, pp. 2842-2844.

Chan, S., et al, "Building Parallelism into the Instruction Pipeline", High Performance Systems, Dec., 1989, pp. 53-60.

Murakami, K, et al, "SIMP (Single Instruction Stream/Multiple Instruction Pipelining); A Novel High-Speed Single Processor Architecture", Proceedings of the Sixteenth Annual Symposium on Computer Architecture, 1989, pp. 78-85.

Smith, J. E., "Dynamic Instructions Scheduling and the Astronautics ZS-1", IEEE Computer, Jul., 1989, pp. 21-35.

Smith, M. D., et al, "Limits on Multiple Instruction Issue", ASPLOS III, 1989, pp. 290-302.

Tomasulo, R. M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units", Computer Structures, Principles, and Examples (Siewiorek, et al ed), McGraw-Hill, 1982, pp. 293-302.

Wulf, P. S., "The WM Computer Architecture", Computer Architecture News, vol. 16, No. 1, Mar. 1988, pp. 70-84.

(List continued on next page.)

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[57] ABSTRACT

A digital computer system is described which is capable of processing 2 or more computer instructions in parallel and which has the capability of generating compounding tag information for those instructions, the compounding tag information being associated with instructions for the purpose of indicating groups of instructions which are to be concurrently executed. A compounding tag has a value which indicates the size of the group of instructions which are to be concurrently executed. The computer system includes a hierarchially-arranged memory which provides instructions to a CPU for execution. The instructions are compounded in the memory, and provision is made in the memory for storage of their compounding tags. In the event of modification of an instruction in memory, the invention provides for reduction of the value of the compounding tags for the modified instruction and instructions which are capable of being compounded with the modified instruction or for generation of new tag values for the modified instruction and instructions which are adjacent it in memory.

15 Claims, 15 Drawing Sheets